



04-16-04

Express Mail No. EV331754605US
Attorney Docket No. UMI-359
Client/Matter No. 80450.0090

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Kim C. Hardee

Serial No. 10/776,054

Filed: February 11, 2004

For: COLUMN READ AMPLIFIER POWER-GATING
TECHNIQUE FOR INTEGRATED CIRCUIT
MEMORY DEVICES AND THOSE DEVICES
INCORPORATING EMBEDDED DYNAMIC
RANDOM ACCESS MEMORY (DRAM)

Group Art Unit: Not Yet
Assigned

Examiner: Not Yet Assigned

Confirmation No.: Not Yet
Assigned

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits for filing under 37 CFR 1.97 a disclosure statement. In submitting this reference, no representation is made or implied that the reference is or is not material to the examination of this application. The patents, publications or other information of which Applicant is presently aware are listed in Form PTO/SB/08A submitted herewith and copies of all such patents and publications are attached hereto.

No fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

14 Apr 2004
Date

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Application Number	10/776,054
				Filing Date	February 11, 2004
				First Named Inventor	Kim C. Hardee
				Art Unit	Not Yet Assigned
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket No.	UMI-359

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher, city and/or country where published	T ²
		MIN, KYEONG-SIK, KAWAGUCHI, HIROSHI, SAKURAI, TAKAYASU, ZigZag Super Cut-off CMOS (ZSCCMOS) Block Activation with Self-Adaptive Voltage Level Controller: An Alternative to Clock-Gating Scheme in Leakage Dominant Era, 2003 IEEE International Solid-State Circuits Conference, February 12, 2003, Salon 1-6, pp. 400-401 and 501-502.	

EXAMINER SIGNATURE		DATE CONSIDERED	
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			
¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) and application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.			



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CERTIFICATE OF MAILING BY EXPRESS MAIL

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Sir:

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2. Form PTO/SB/08A, with reference;
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relating to the above application, were deposited as "Express Mail" Mailing Label No. EV331754605US, with the United States Postal Service, addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 15 April 2004.

15 April 2004

Date

19 April 2004

Date

Maier

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